IN THE CLAIMS

1. (Currently Amended) A method of checking the accuracy of a pseudorandom bit sequence (PRBS) ~~received by a device~~, wherein a first PRBS is generated at a PRBS generator, comprising a first shift register chain, and presented to a device under test, and the device under test generates a second PRBS in response to the first PRBS, the method comprising the steps of:

delaying the second PRBS ~~received by the device~~ in a second shift register chain that corresponds to the first shift register chain to generate a delayed second PRBS;

detecting the presence of an error bit in the second PRBS ~~received by the device~~ by comparing ~~at least a portion of~~ the delayed second PRBS at an intermediate point in the second shift register chain with ~~at least a portion of~~ the second PRBS ~~received by the device~~; and

prohibiting propagation of the detected error bit ~~in the delayed PRBS~~ such that the detected error bit does not further propagate through the second shift register chain[[;]] .

~~wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.~~

2. (Currently Amended) The method of claim 1, wherein the prohibition step serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the second PRBS ~~received by the device~~.

3. (Original) The method of claim 1, wherein the prohibition step further comprises correcting the error bit.

4. (Currently Amended) The method of claim 1, further comprising the step of detecting the non-presence of a PRBS from the device under test.

5. (Currently Amended) The method of claim 1, wherein the device under test is one of a communication circuit and a communication channel.

6. (Currently Amended) Apparatus for checking the accuracy of a pseudorandom bit sequence (PRBS) ~~received by a device~~, wherein a first PRBS is generated at a PRBS generator, comprising a first shift register chain, and presented to a device under test, and the device under test generates a second PRBS in response to the first PRBS, the apparatus comprising:

a memory; and

at least one processor coupled to the memory and operative to: (i) delay the second PRBS ~~received by the device~~ in a second shift register chain that corresponds to the first shift register chain to generate a delayed second PRBS; (ii) detect the presence of an error bit in the second PRBS ~~received by the device~~ by comparing ~~at least a portion of~~ the delayed second PRBS at an intermediate point in the second shift register chain with ~~at least a portion of~~ the second PRBS ~~received by the device~~; and (iii prohibiting propagation of the detected error bit ~~in the delayed PRBS~~ such that the detected error bit does not further propagate through the second shift register chain[[;]] ~~wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device~~ .

7. (Currently Amended) The apparatus of claim 6, wherein the prohibition operation serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the second PRBS ~~received by the device~~.

8. (Original) The apparatus of claim 6, wherein the prohibition operation further comprises correcting the error bit.

9. (Currently Amended) The apparatus of claim 6, wherein the processor is further operative to detect the non-presence of a PRBS from the device under test.

10. (Currently Amended) The apparatus of claim 6, wherein the device under test is one of a communication circuit and a communication channel.

11. (Currently Amended) An article of manufacture for checking the accuracy of a pseudorandom bit sequence (PRBS) ~~received by a device~~, wherein a first PRBS is generated at a PRBS generator, comprising a first shift register chain, and presented to a device under test, and the device under test generates a second PRBS in response to the first PRBS, the article comprising a machine readable medium containing one or more programs which when executed implement the steps of:

delaying the second PRBS ~~received by the device~~ in a second shift register chain that corresponds to the first shift register chain to generate a delayed second PRBS;

detecting the presence of an error bit in the second PRBS ~~received by the device~~ by comparing ~~at least a portion of~~ the delayed second PRBS at an intermediate point in the second shift register chain with ~~at least a portion of~~ the second PRBS ~~received by the device~~; and

prohibiting propagation of the detected error bit ~~in the delayed PRBS~~ such that the detected error bit does not further propagate through the second shift register chain[[;]] .

~~wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.~~

12. (Currently Amended) Apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device under test in response to an input PRBS received by the device under test from a PRBS generator comprising a first shift register chain, the apparatus comprising:

a second shift register chain that corresponds to the first shift register chain;

a logic gate coupled to the second shift register chain and the device under test for detecting, for a given clock cycle, the presence of an error bit in the output PRBS generated by the device under test, the error bit representing a mismatch between the input PRBS generated by the PRBS generator and the output PRBS generated by the device under test; and

at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the second shift register chain.

13. (Currently Amended) The apparatus of claim 12, further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS generated by the PRBS generator to pass through the device under test and initialize the full length of the second shift register chain.

14. (Original) The apparatus of claim 13, wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector.

15. (Currently Amended) The apparatus of claim 12, further comprising an error counter coupled to the logic gate for counting errors detected between the input PRBS generated by the PRBS generator and the output PRBS generated by the device under test.

16. (Original) The apparatus of claim 15, further comprising an error count display coupled to the error counter for displaying the error count.

17. (Currently Amended) The apparatus of claim 12, further comprising a third logic detector coupled to the second shift register chain for detecting the non-presence of a PRBS from the device under test.